Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A device for extending address space by inserting a waiting state, wherein the device is coupled to an external memory through a bus, and the external memory has stored at least a first program, the device comprising:
a read-only memory (ROM), for storing a second program;
a central processing unit (CPU), coupled to the ROM, for executing the first program or the second program; and
a memory interface controller, for inserting a waiting state into the CPU when the CPU intends to execute an instruction of the first program stored in the external memory.

[c2] 2. The device of claim 1, wherein the device is a microcontroller.

[c3] 3. The device of claim 1, wherein the memory interface controller comprises:
a memory interface, coupled the bus, serving as a transmission interface between the memory interface controller and the bus;
a range checking unit, used to judge whether or not an address of an information, which is to be accessed by

the CPU, is located within a predetermined range, and selectively issuing a range checking signal; and
a state control unit, coupled to the memory interface, the range checking unit, and the CPU, used for inserting the waiting state into the CPU when the range checking signal is received.

[c4] 4. The device of claim 3, wherein the range checking unit issues the range checking signal when the address of the information to be accessed by the CPU is located within an address range of the external memory or out of an address range of the ROM.

[c5] 5. The device of claim 3, further comprising an inquiry mode, and the memory interface controller further comprising:
a buffer, coupled to the memory interface, for temporarily store the information accessed from the external memory through the bus; and
a ready flag, coupled to the buffer and the CPU, wherein the CPU inquires the ready flag, and the CPU correctly accesses the information through the buffer when buffer has correctly accessed the information of the external memory through the memory interface.

[c6] 6. The device of claim 5, wherein when the CPU sets the device to the inquiry mode, the state control unit does

not insert the waiting state into the CPU, and memory interface controller is activated by executing a read memory instruction.

[c7] 7. The device of claim 5, wherein the buffer includes a plurality of registers, the registers can store at least one byte information set.

[c8] 8. The device of claim 5, wherein the accessed information by the inquiry mode includes voice information or music information.

[c9] 9. The device of claim 1, wherein a transmission unit in one time is one bit, two bits, one nibble, or one byte.

[c10] 10. The device of claim 3, wherein the predetermined address range can be freely set.

[c11] 11. An operation method on a device for extending address space by inserting a waiting state, wherein the device at least includes a central processing unit (CPU), the operation method comprising:
setting a predetermined address range;
judging whether or not an address of a program instruction to be fetched is located within the predetermined address range;
inserting a waiting state into the CPU when the address is located out of the predetermined address range, until

the program instruction is completely fetched; and executing the program instruction by the CPU.

[c12] 12. The operation method of claim 11, wherein the device is a micro-controller.

[c13] 13. The operation method of claim 11, wherein the waiting state being inserted into the CPU cause a clock state of the CPU to remain.

[c14] 14. The operation method of claim 11, wherein predetermined address range can be freely set.